



NAME Lee, Seong-Min
 Position Professor
 Phone +82+32-835-8276
 Office 8-306
 E-mail smlee@inu.ac.kr
 Homepage <http://mse.inu.ac.kr>

Degree	<ul style="list-style-type: none"> • 1983 B.E. : Hanyang University, Engineering • 1986 M.S. : University of Wisconsin-Madison, Engineering • 1993 Ph.D. : University of Wisconsin-Madison, Engineering
Experience	<ul style="list-style-type: none"> • 1998~Present Univ. of Incheon, Assistant Professor, Associate Professor, Professor • 2005~2006 MIT, Visiting Professor • 1994~1997 Samsung Electronics, Senior Researcher • 1993~1994 University of Wisconsin-Madison, Post Doctor
Major	<ul style="list-style-type: none"> • Micro-electronic Packaging
Teaching	<ul style="list-style-type: none"> • Physical Chemistry of Materials, Materials Mechanics, Semiconductor Assembly
Representative Research	<ul style="list-style-type: none"> • Adoption of Single-Sided Adhesive tape to Improve Thermal-Cycling Reliability in Semiconductor Devices, Current Applied Physics, Vol. 11, pp. S396 (2011) • Effect of Grinding-Induced Scratch Geometry on Fracture Strength of Semiconductor Devices, Surface Review & Letters, Vol. 17, No 3, pp.1 (2010)
Researches	<ul style="list-style-type: none"> • A Effect of Grain Size Evolution in Au-Wire Ball on Debonding Failure with Al-Pad in Semiconductor Devices, Thin Solid Films, Vol. 641, pp.69 (2017) • Effect of Sub-Micro or Nano-Scale Defects Resulting from Various Wafer Finishing Processes on Degradation--, J. of Nanosci. & Nanotech., Vol.17, pp.7830 (2017) • Adoption of Hybrid Dicing Technique to Minimize Sawing-Induced Damage, The Japan Institute of Metals and Materials, Vol. 58, No. 4, pp. 530 (2017). • Dependence of Chipping Damage on Crystallographic Orientation during Mechanical Dicing of Silicon Wafers, J. of Nanoscience & Nanotechnology, Voi. 16, pp.1 (2016) • Effect of Sawing Velocity Variation on Chipping Damage of Semiconductor Wafers with Different Thickness, KJMM, Vol. 54, No. 8, pp.598 (2016) • Effect of Polishing Process of Semiconductor Wafer on Fracture Mechanics of Diced Chips, KJMM, Vol. 54, No. 3, pp.204 (2016) • Effect of Sawing Velocity Variation on Mechanical Dicing-Induced Damage in Semiconductor Silicon Wafer, KJMM, Vol. 53, No. 5, pp.306 (2015) • Advanced LOC Tape Design to Improve Thermal-Cycling Reliability in Semiconductor Devices, Science of Advanced Materials, Vol. 6, pp.1 (2014)
Current Research	<ul style="list-style-type: none"> • Design of 3-Dimensional Microelectronic Packages • Reliability Improvement of Plastic-Encapsulated Microelectronic Packages